CLAIMS

1. A photo mask set comprising:

a first photo mask having a plurality of parallel lower opaque patterns formed on a first transparent substrate, wherein the ends of the lower opaque patterns are located on a straight line; and

a second photo mask having a plurality of upper opaque patterns formed on a second transparent substrate, the upper opaque patterns positioned to overlay the lower opaque patterns.

2. The photo mask set of claim 1, wherein at least one of the upper opaque patterns extends past the end of a corresponding lower opaque pattern.

3. A photo mask set comprising:

a first photo mask having a plurality of parallel lower opaque patterns formed on a first transparent substrate, the lower opaque patterns comprising a first lower opaque pattern, a second lower opaque pattern, and a third lower opaque pattern located between the first and second lower opaque patterns, the first and second lower opaque patterns extending past an end of the third lower opaque pattern; and

a second photo mask having a first upper opaque pattern, a second upper opaque pattern, and a third upper opaque pattern formed on a second transparent substrate, the first, second, and third upper opaque patterns positioned to overlap with the first, second, and third lower opaque patterns, respectively.

4. The photo mask set of claim 3, the second photo mask further comprising a fourth upper opaque pattern extending along the same line as the third upper opaque pattern but separated from it by a distance, the distance being greater than a maximum focus distance.

5. A photo mask set comprising:

a first photo mask having a plurality of parallel lower opaque patterns formed on a first transparent substrate, the lower opaque patterns including a first lower opaque pattern, a second lower opaque pattern, and a third lower opaque pattern located between the first and

second lower opaque patterns, the first and second lower opaque patterns extending past an end of the third lower opaque pattern; and

a second photo mask having a first upper opaque pattern and a second upper opaque pattern formed on a second transparent substrate, the first and second upper opaque patterns positioned to overlap with the first and second lower opaque patterns, respectively.

6. The photo mask set of claim 5, wherein the second photo mask further comprises a third upper opaque pattern formed to overlap with the third lower opaque pattern, the third upper opaque pattern extending past an end of the third lower opaque pattern, wherein a predetermined region of the third upper opaque pattern that extends past the end of the third lower opaque pattern is wider than the rest of the third upper opaque pattern.

7. A semiconductor device having multi-layered interconnection lines comprising:

a plurality of lower interconnection lines formed to be parallel in a single direction on a semiconductor substrate, the lower interconnection lines each having an end aligned with each other on a straight line;

an interlayer insulating layer covering an entire surface of the substrate having the lower interconnection lines; and

a plurality of upper interconnection lines formed to overlap with the lower interconnection lines on the interlayer insulating layer.

8. The semiconductor device of claim 7, wherein the upper interconnection lines extend past the ends of the lower interconnection lines.

9. The semiconductor device of claim 7, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

10. The semiconductor device of claim 7, wherein the interlayer insulting layer is formed with at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

11. The semiconductor device of claim 7, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

12. A semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

a plurality of parallel lower interconnection lines formed on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer formed on an entire surface of the substrate having the lower interconnection lines; and

a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line formed on the insulating layer, the first, second, and third upper interconnection lines overlapping the first, second, and third lower interconnection lines, respectively.

13. The semiconductor device of claim 12, further comprising:

a fourth upper interconnection line formed on the insulating layer and located on the same line as the third upper interconnection line but separated from it by a distance, the distance between the third and fourth upper interconnection lines being greater than a longest focus distance.

14. The semiconductor device of claim 12, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

15. The semiconductor device of claim 12, wherein the interlayer insulting layer comprises at least one layer selected from the group consiting of BPSG, USG, PSG, SOG and PE-TEOS.

16. The semiconductor device of claim 12, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

17. A semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

a plurality of parallel lower interconnection lines formed on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer formed on an entire surface of the substrate having the lower interconnection lines; and

a first upper interconnection line and a second upper interconnection line formed on the insulating layer, the first and second upper interconnection lines overlapping the first and second lower interconnection lines, respectively.

18. The semiconductor device of claim 17, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

19. The semiconductor device of claim 17, wherein the interlayer insulting layer comprises at least one layer selected from a group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

20. The semiconductor device of claim 17, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

21. A method for forming multi-layered interconnection lines in a semiconductor device, the method comprising:

forming a lower interconnection line on the semiconductor substrate;

forming an interlayer insulating layer on the substrate and the lower interconnection line;

forming a conductive layer on the interlayer insulation layer;

determining a slope profile of the conductive layer;

forming a photoresist layer on the conductive layer; and

forming an upper interconnection line using a photolithography process that includes a photo mask based on the slope profile.

22. The method of claim 21, wherein forming the upper interconnection line comprises forming an upper interconnection line over the lower interconnection line in a region of the photoresist layer where light from the photolithography process is not reflected.